FACULTY OF ENGINEERING

B.E. III/IV Year (ECE) I Semester (Main) Examination, November/December 2008
(New)

COMPUTER ORGANIZATION AND ARCHITECTURE

Time : 3 Hours] [Max. Marks : 75

Answer all questions from Part A.
Answer any five questions from Part B.

Part A — (Marks : 25)

1. Explain the memory operation of the following transfer statements.
   (a) R2 ← M [AR]
   (b) M[AR] ← R3
   (c) R5 ← M[R5]

2. Specify the sequence of micro operations that will perform the following operations in a basic computer
   IR ← M[AC]
   AC ← AC + TR
   DF ← DF + AC

3. Give the instruction format of a basic computer the memory, register and I/O reference instructions.

4. Draw the Block diagram of a 4-bit binary incremeneter.

5. Differentiate between internal and external interrupts.

6. Give the no. of memory references, when w fetches and executes an indirect addressing mode instruction if instruction is
   (a) Computational type requiring an operand from memory
   (b) a branch type

7. Explain the need for an I/O interface.

8. Differentiate between an isolated I/O and memory mapped I/O.

9. Explain the concept of virtual memory.

10. Explain the terms Tag, Index and Block in relation to cache memory.

[P.T.O.]
Part B — (Marks: 50)

11. (a) Explain addition/subtraction of floating point numbers with necessary flow chart.
      (b) Draw a 4-bit combinational circuit shifter and explain.

12. (a) Explain the phases of an instruction cycle with necessary control functions and
        micro operations.
     (b) Differentiate between Hard wired and micro-programmed control unit.

13. (a) Explain 4 possible Hardware schemes that can be used in an instruction pipe-
        line in order to minimize the performance degradation caused by instruction
        branching.
    (b) An instruction is stored at location 300H with its address field at location 301H.
        Address field has a value 400H. A process register contains 200H. Evaluate
        effective address if the address mode of instruction is
           (i) Index with R1             (ii) relation                (iii) Register indirect

14. (a) Draw and explain the block diagram of an asynchronous communication
        interface.
   (b) Explain polling and Daisy chain priority interrupt-initiated I/O mode of data
        transfer.

15. (a) Explain segmented page mapping technique with the help of a numerical example.
      (b) Explain Association memory with a neat block diagram and derive the match
           logic for one word of association memory.

16. (a) Explain address sequencing for a micro programmed control with a neat block
        diagram.
   (b) Explain Auto increment/decrement mode of addressing.

17. Write short notes on:
   (a) Magnetic disks
   (b) Multiprocessor
   (c) IOP-CPU communication.