FACULTY OF ENGINEERING

B.E. III/IV Year (ECE) I Semester (Main) Examination, November 2007

COMPUTER ORGANIZATION AND MICROPROCESSORS

Time : 3 Hours] [Max. Marks : 75

Answer all questions of Part A.
Answer five questions from Part B.

Part A – (Marks : 25)

1. How does a Microprocessor differentiate between data and Instruction? 2
2. What are the basic elements of floating point addition and subtraction. 3
3. How are data read from and written onto a magnetic disk. 3
4. Distinguish between memory mapped I/O, and I/O mapped I/O, how many I/O devices can be addressed in each case. 3
5. Define Instruction cycle, machine cycle and T-state. 3
6. What is the function of ALE signal of 8085 microprocessor. 3
7. What is the result of the following program segment
   MVIA, OCH
   SIM
2
8. Find the error and correct the following instruction
   ADD DS #0030H
   ROR BX, CX
2
9. Mention the functions of an Assembler. 2
10. List the features of RISC Machines. 2

Part B – (Marks : 5 × 10 = 50)

11. (a) Explain the stock organisation of a computer with an example. 6
(b) Explain about the basic components of computer. 4

12. (a) What are the differences among direct mapping, associative mapping and set-associative mapping? 6
(b) What are the various functions of I/O module? 4

[P.T.O.]
13. (a) Write an ALP for 8085 to add two multiprecision BCD numbers.
(b) Explain “CALL Addr” Instruction with timing diagram.

14. (a) Explain the function of the following pins of 8085
(ii) ALE (ii) IO/ M (iii) S0, S1 (iv) SID and SOD.
(b) Draw the machine cycle diagram and explain the instruction.
MOV A1 M.

15. (a) Explain with a neat diagram how a matrix keyboard is interfaced to 8085
write a program to read a key pressed.
(b) Interface an 8-bit DAC to 8085 through PA8255 write an ALP to generate a
square waveform with 100 μsecond time period.

16. (a) Show the block schematic diagram of 8253 PIT chip and explain any three
modes of its operation.
(b) Design and draw a memory interface circuit to an 8085 CPU bus to meet the
following specifications using 4K × 8 bits SRAM chips
(i) 8k bytes of ROM area starting OOOOH
(ii) 8k bytes of SRAM area starting 8000H.

17. (a) Compare RISC and CISC Processors.
(b) Write about array processors.