FACULTY OF ENGINEERING
B.E. 3/4 (ECE) I-Semester Main Examination, November, 2004
(For Backlog Students)

Subject: COMPUTER ORGANISATION & ARCHITECTURE

Time: 3 Hours
Max. Marks: 75

N.B: Answer all questions of Part-A and any Five questions from Part-B.

PART - A (25 Marks)

1. A 36-bit floating point binary number has 8 bits plus a sign for the exponent. The Mantissa is assumed to be a normalized fraction. Negative numbers in the Mantissa and exponent are in signed-magnitude representation. What are the largest and smallest positive quantities that can be represented excluding zero?

2. Design a 4-bit arithmetic circuit with one select variable 'S' and two 4-bit data inputs 'A' and 'B'. When S=0, the circuit performs the addition A+B, when S=1, the circuit performs A-B by 2's complement of 'B'.

3. Under what conditions would it be more feasible to use a hard wired control than a microprogrammed control unit?

4. List the advantages and disadvantages of memory mapped compared to isolated I/O.

5. A DMA module is transferring characters to memory using cycle-stealing, from a device transmitting at 9600 bps. The CPU is fetching instructions at the rate of 1 million instructions per second. By how much will the processor be slowed down due to the DMA module?

6. Draw a flow chart for Booth's multiplication algorithm.

7. Explain the importance of Associative memory and its operation.

8. Describe how the multiple interrupts are being serviced?

9. Brief the services typically provided by an operating system.

10. Compare RISC and CISC machines.

PART - B (5x10=50 Marks)

11. Draw the logic diagram of a 4-bit register with clocked JK flip flops having control inputs for the increment, complement, and parallel transfer micro-operations. Show how the 2's complement can be implemented in this register?

12. It is possible to reduce the time it takes the control to process a register reference instruction in the basic computer. Show that if the register-reference instructions are executed with timing variable t3 during the 'fetch cycle', the control will process them in half the time it now takes. Show the register transfer relations for the fetch cycle that will take care of this proposed change.

13. Explain various types of Instruction formats and addressing methods employed in a general purpose computer with examples.
14. Show how a 9-bit micro operation field in a micro instruction can be divided into subfields to specify 46 micro operations. How many micro-operations can be specified in one micro-instruction? Mention the applications of Micro-programming.

15. What is meant by locality of reference in memory systems? Explain mapping, store through, load through and replacement algorithms with reference to Cache-memory.

16. What are the scheduling strategies followed in an O.S. in a multiprocessor environment?

17. Write short notes on:
   a) Stack organisation
   b) Assemblers.